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Real-time power switch fault diagnosis and fault-tolerant operation in a DFIG-based wind energy system

Mahmoud Shahbazi, Philippe POURE and Shahrokh SAADATE

Abstract

As wind energy production increases, reliability and fault-tolerant operation capability of wind energy systems are becoming more important. Modern wind energy production systems use power electronic converters which are unfortunately proved to be one of their most fragile parts and responsible for most of the system downtime. Real-time fault monitoring, fault diagnosis and proper system reconfiguration in these converters are therefore mandatory for fault-tolerant operation of the converter and the whole system. In this paper, a comprehensive fault-tolerant power electronics interface for wind energy systems with doubly-fed induction generators is presented and validated. The same power production capability will be guaranteed. The proposed solution also includes a robust and very fast open-circuit switch fault diagnosis algorithm, which is not sensitive to the operation conditions and is therefore suitable for this application. Simulation, Hardware in the Loop validation and experimental tests are carried out to demonstrate the effectiveness of the proposed approach.

Keywords: Power switch fault diagnosis, fault tolerant operation, wind energy, Doubly-fed induction generator

1. Introduction

Wind energy production has been growing rapidly in the recent years. However, with the ever increasing use of wind turbines, many challenges have also appeared. In most cases, the wind turbines are installed in remote areas where their maintenance is costly and time-consuming. Therefore, the reliability of Wind Energy Conversion Systems (WECS) is of paramount importance. On the other hand, Power Electronic (PE) converters are proved to be one of the most fragile parts of a WECS. The proportion of maintenance cost for these devices is high, and they are responsible for approximately 14% of the total downtime of wind turbines [1]. Another study [2] shows that frequency converters cause the longest downtime in the wind farms, being responsible for more than 22% of the overall downtimes. All these data show the importance of their reliability and the usefulness of the continuity of service of these converters, especially considering the fact that such downtimes directly result in financial losses.

When reliability is of major concern, Fault Tolerant Systems (FTS) also become important. Such systems provide the possibility of balanced and controlled operation of the system even after a fault occurrence and therefore preventing operation interrupts. Therefore, in recent years fault tolerant control and Fault Diagnosis (FD) of wind turbines have gained much attention. For example, detection of debris build-up on the wind turbine blades, misalignment of one or more blades and change in the drive train damping due to wear and tear are investigated in [3] and a fault detection problem is tackled using interval nonlinear parameter-varying parity equations. Generator output power and rotational speed of the wind turbine are used in [4] to derive a fault detection signal using a continuous-wavelet-transform-based adaptive filter. Both electrical and mechanical faults were successfully detected. Faults in sensors are investigated in [5-7], considering position, current and voltage sensor faults. Detection of wind turbine drive train faults, including the damage detection of blades through the terminals of the generator is investigated in [8]. A review of many condition monitoring algorithms for different parts of WECSs is presented in [9].

Many papers in the recent years have studied fault tolerant operation of power electronic converters in general applications such as electrical drives. For example, several fault-tolerant techniques for two-level and multilevel converters are reviewed in [10]. Another survey of condition monitoring and fault-tolerant operation for electric machines and drives is available in [11]. A fault-tolerant control strategy for a T-type three-level inverter under open-circuit fault conditions is proposed in [12]. No additional components are required, but the inverter operation without output distortions is possible with reduced power at reduced output voltage. Few studies have specifically aimed the converters in WECSs, where most of them have been focused on Permanent Magnet Synchronous Generator (PMSG)-based systems. In [13], a fault-tolerant topology for post-fault operation of the grid side converter of a PMSG-based system is proposed which is based on a five-leg converter with the shared leg connected to a phase of the generator and to the transformer's neutral point. Another method presented in [14] proposes to connect the output phases to the middle point of the DC link after fault detection, but in this structure the grid-side converter switches will experience two times bigger voltage in the post-fault mode which reduces its practicality. In [15], a fault-tolerant control for open-switch faults in three-level NPC converters of PMSG-based systems is proposed that used d-axis current injection to eliminate current distortion in the post-fault operation mode.

The authors of [16, 17] have studied the fault in the converter in a Doubly-Fed Induction Generator (DFIG) and the reconfiguration after fault diagnosis. A fault-tolerant PE structure is proposed in [18] which is developed by replacing the conventional six-switch Grid Side Converter (GSC) with a nine-switch alternative. While the proposed system is designed to address grid faults, converter faults are not considered. Current sensor faults are investigated in [19] and a new current observer is used for improved current sensor fault detection. Faults such as those in generator speed sensor and pitch subsystem are considered in [20] where an observer based active fault-tolerant control approach is proposed.

1 In all fault-tolerant systems, fault detection is the foremost step. The presence of a fault or
2 malfunction in the system must be quickly detected, as well as its location. In recent years,
3 many publications have addressed the fault diagnosis methods, including a number of high
4 quality surveys. For example, in [21, 22] a survey of fault diagnosis and fault-tolerant
5 techniques including fault diagnosis with model-based, signal-based, knowledge-based and
6 hybrid/active approaches for a variety of applications including power electronic converters
7 is presented. More particularly many methods are available for fault diagnosis in power
8 switches in power electronic converters. For example, the fault diagnosis algorithm for a
9 conventional three-phase converter presented in [23] is based on the recognition of Park's
10 normalized current space vector trajectory. Some papers have specifically targeted the power
11 converters in WECSs. Open switch fault in variable speed situations is studied in [24] where
12 some of the existing fault detection methods are also investigated for this application. It is
13 shown that many of the existing fault diagnosis methods including those based on Park's
14 vector approach may experience problems in variable wind speeds or in turbulent wind
15 situations. Moreover, many of the current based methods experience problems in very low
16 frequency currents. On the other hand, DFIG-based turbines are one of the most used
17 structures of wind turbines due to the smaller PE rating. In these systems, rotor current can
18 be quite low around the synchronous speed and therefore many of the existing fault
19 detection algorithms are expected to be not efficient in detecting the fault, or even
20 completely unable to detect the fault. However, in [17], a modified method is presented that
21 takes the low frequency nature of rotor current into account. Still, the fault detection is
22 relatively slow, and is not practically validated.

23 In this paper, a fault tolerant converter for a DFIG-based WECS is proposed; it is capable of
24 very fast open-circuit switch fault diagnosis and proper reconfiguration in order to guarantee
25 the seamless operation of the whole system. The employed fault diagnosis algorithm uses
26 voltage rather than current measurement, and therefore is resilient against very low
27 frequency rotor currents. Moreover, it is very fast and minimizes the adverse effects of the
28 fault on the drive train, and the fault detection time does not depend on wind or load
29 conditions.

30 On the other hand, a fault tolerant system could be with or without hard redundancy. If some
31 level of degraded operation is acceptable, then a system without hard redundancy might be
32 enough. For example, [25] presents a DFIG system without redundancy, where the power
33 electronic interface is reconfigured after a switch fault occurrence to continue with the
34 remaining 5 healthy legs. However, in such systems, the power handling capability of the PE
35 converters is quite reduced. Moreover, in such a system the total phase current of both sides
36 of the converter passes through the common leg after reconfiguration, therefore all switches
37 should be overrated to be capable of handling this current. More importantly, the dc-link
38 voltage in this case may be quite higher than in the pre-fault case; therefore special attention
39 must be paid to the control of the converters as well as to their design in the conception stage.

In this paper, however, a quite efficient solution is presented which only needs two additional switches, but enables full rated operation in post fault situations. Moreover, the control system remains unchanged after fault diagnosis and reconfiguration.

The rest of the paper is organized as follows: in section 2, the proposed fault tolerant structure, the topology and the fault diagnosis algorithm are presented. A rapid prototyping scheme including Hardware-In-the-Loop (HIL) verification is explained and used for evaluating the proposed system. Experimentations are carried out in section 3 in order to validate the proposed approach. Finally, some conclusions are provided.

2. Proposed fault-tolerant system

2.1. The topology

Fig. 1 shows the DFIG-based WECS incorporating the fault-tolerant converter. The fault tolerant converter is in fact a back-to-back converter including an additional leg that can replace any of the other legs in case of a fault in them. This is realized using six bidirectional switches which can connect the output of the redundant leg to all input and output phases of the converter. Triacs are used to realize these bidirectional switches.

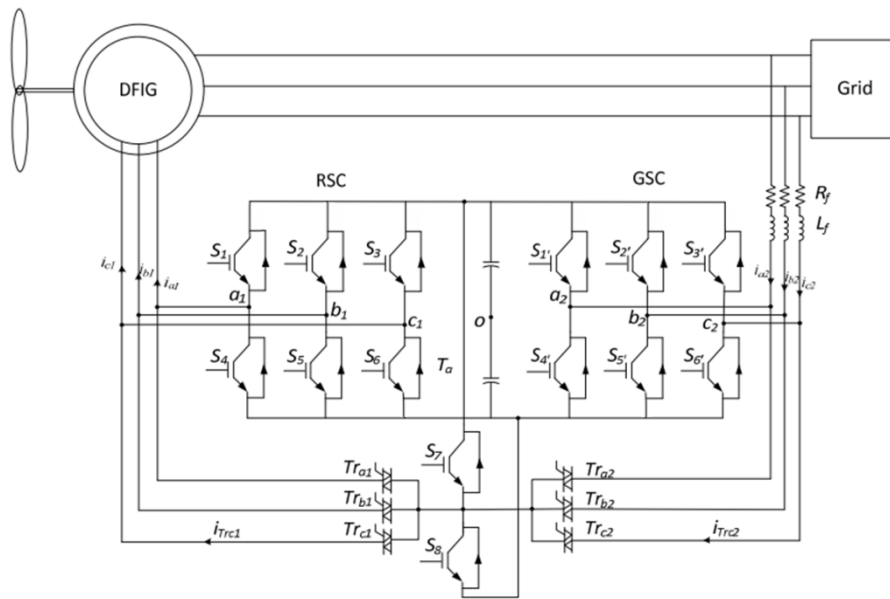


Fig. 1. The fault-tolerant DFIG-based WECS.

The DFIG can be controlled by applying proper voltages via the Rotor Side Converter (RSC). Many methods are available in the literature, but a widely used and well known method is vector control using Park transformation. Using proper decoupling terms, d and q currents can be controlled to control the stator flux and output torque respectively. The GSC is used for controlling the DC link voltage, and also the AC side power factor which is here set to unity. In this work, the voltage-based control method of [26] is used to calculate the reference

voltages of the PWM unit of this converter. Fig. 2 shows the block diagram of the RSC control. Q_s^* stands for the reference of the stator reactive power, T_e^* is the reference for electromagnetic torque of the DFIG, φ_s is the stator flux, and i_r and v_r are rotor current and voltage respectively. Subscripts 'd' and 'q' represent the variable in 'd' and 'q' coordinates of the Park transformation. ω_r is the frequency of rotor waveforms, L_s , L_m and L_r are total stator inductance, magnetizing inductance and total rotor inductance respectively.

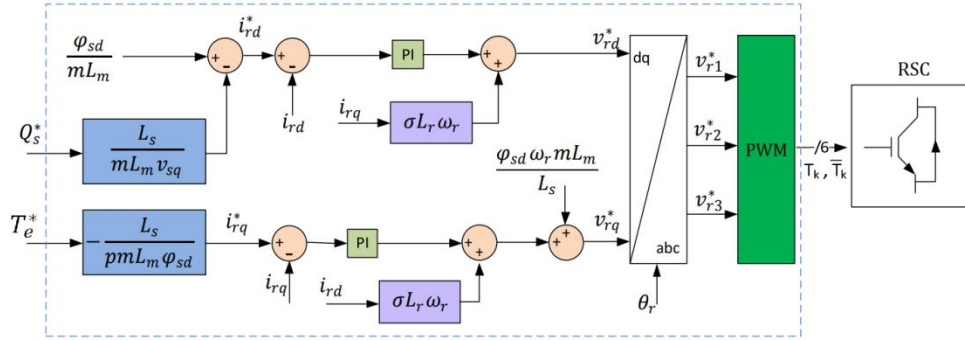


Fig. 2. Block diagram of the control of rotor voltages and currents.

2.2- Open-circuit switch fault diagnosis algorithm

In all fault-tolerant systems, fault diagnosis is the foremost step. Here a fault diagnosis method is used that is based on voltage rather than current measurement. Combined with a proper hardware implementation, this method which is very fast compared to other existing fault diagnosis methods, minimizes the effect of a fault on the system. More importantly, this method is independent of the system parameters as well as wind conditions, which makes it more resilient and better-suited for fault-tolerant operation.

Fig. 3 shows the fault detection block diagram.

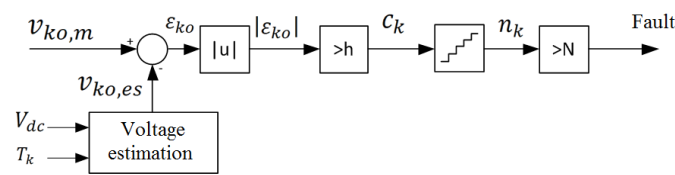


Fig 3. The fault detection block diagram.

The fault detection method is based on direct comparison of the measured and estimated pole voltages. Estimated voltages are formed from each leg's switching commands and the DC link voltage through eq.1. DC-link voltage is anyways measured for control and monitoring purposes, and switching commands are calculated in the controller and are therefore available.

$$V_{ko,es} = \frac{(2T_k - 1) \times V_{dc}}{2} \quad (1)$$

Where $T_k \in \{0,1\}$ is the switching command applied to the upper switch of leg 'k' ($k \in \{a_1, b_1, c_1, a_2, b_2, c_2\}$ -see Fig.1). The command of lower switch is complementary of the upper one to avoid short circuit and provides a current path. $V_{ko,es}$ is the estimated pole voltage with reference to the middle point of the DC-link capacitor. The difference between the estimated and measured voltages contains information on the health of the leg's switches. In normal mode of operation and in an ideal converter, this difference is negligible. In reality, however, uncertainties and disturbances should be considered as well. In fact, they are present in the estimation and measurement parts of the system. The estimation is not ideal, partly due to the delays and dead-times in the converters, including the switching turn-on and turn-off delays, and also due to the measurement and discretising errors in measuring V_{dc} . The measurement of pole voltages ($V_{ko,m}$) also suffers from these errors. Due to the aforementioned delays, the difference between the measured and estimated voltages during switching intervals can reach $\frac{V_{DC}}{2}$, but for very limited time spans. During other times, there still might be a little difference between measured and estimated voltages due to the mentioned measurement and discretising errors. Therefore, in the fault diagnosis algorithm, the absolute value of the voltage error is first compared to a threshold value of 'h', which is chosen appropriately to filter the measurement and quantization errors (Fig.3). The value of 'h' is chosen equal to $V_{DC}/4$ here, which is normally several times larger than the mentioned errors in normal operation, yet smaller than the voltage error in faulty operation mode. Afterwards, if the voltage error is large enough, its duration is calculated by using a counter. The output of this counter measures the time during which the voltage error has been large enough. This output is again compared to another constant value of N, and therefore voltage errors caused by natural delays and dead-times can be filtered. The overall time that the counter needs to reach N should be adequately larger than the overall delays in the system. When a fault occurs, the voltage error remains large for a long period of time, and therefore the fault can be detected and declared.

3. Evaluation of the proposed FTS and FD algorithm

3.1. FPGA in The Loop" design and prototyping approach

For validation, a rapid prototyping design approach based on a so-called "FPGA in the loop" prototyping method [27] is used in this paper. Fig. 4 shows the associated design flow. In this method, first continuous time simulations in Matlab/Simulink are carried out. Since the control and fault diagnosis are going to be implemented on digital targets, the models are discretised and discrete time simulations are carried out. Following this step, the model system is kept unchanged, but all that is going to be implemented on the digital targets (control and fault diagnosis) are replaced by proper blocks from DSP Builder library, which is a library developed by Altera for implementing designs on their FPGAs. These blocks can be

compiled to VHDL automatically and are therefore suitable for rapid control prototyping and HIL validation. However, some of the more complicated functions may not be available in the library and can be developed in HDL codes and be integrated in the design.

Later on, all DSP Builder blocks can be compiled to produce a single HIL block that represents all those functionalities. This block will then replace all those blocks. Then, FPGA can be programmed using a JTAG interface. At this stage, all the control and FD functions are implemented on the FPGA, while the power system (the turbine, generator, grid and power converters) are simulated in the Matlab/Simulink environment. In each simulation step, the power system sends necessary signals (voltages, currents, etc.) to the FPGA. Control commands and FD signals are then calculated in the FPGA and the necessary data are sent back to Simulink again. In this way, the performance of the controller and FD can be validated experimentally before using them in a real system.

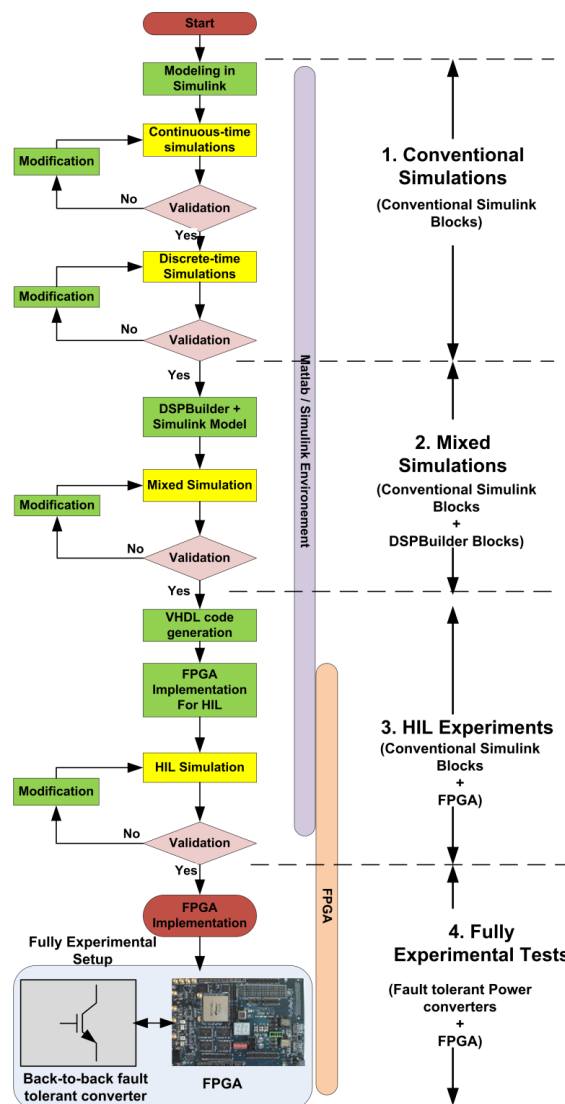


Fig. 4. Rapid prototyping implementation flow.

3.2. Simulation and HIL results

Simulations results are presented here. Table I shows the parameters of the studied system.

Table I. Simulated system parameters.

	Parameters
DFIG	$U_r = U_s = 690 V$ $P_n = 3 MW, f = 50 Hz, p = 2, \frac{N_r}{N_s} \approx 1$ $R_s = 2,97 m\Omega, R_r = 3,82 m\Omega$ $L_s = 12,241 mH, L_r = 12,177 mH$ $L_m = 12,12 mH, J_m = 114 kg.m^2$
DC bus	$C = 38 mF, V_{dc} = 1500 V$
GSC filter	$R_f = 0.075 \Omega, L_f = 0.75 mH$
Electric grid	$U = 690 V, f = 50 Hz$

Simulation step time and sampling rate are equal to $1\mu s$. For fault diagnosis, N is chosen equal to 30. This parameter is related to the delays in the system, and is chosen in accordance with the experimental system that is explained in Section C.

First, an open switch fault is applied to S_3 switch at the RSC (Fig. 1). Fig. 5 shows the stator active and reactive powers before and after fault occurrence, and also the DC-link voltage. Stator reactive power reference has two step changes, before and after fault occurrence, to evaluate the dynamics of the system in pre-fault and post-fault configuration. This figure shows that the fault is properly detected and the topology is reconfigured so that the fault effect is hardly visible, and the WECS can continue producing energy as before. Since the post-fault topology is effectively equivalent to the pre-fault one, the dynamic of the system remains unchanged.

Fig. 6 shows the details of the fault diagnosis. Before fault, the measured and estimated voltages difference is limited to the switching intervals, and therefore the fault counter output has small magnitude. However, after fault, this error will be a high value for a longer period of time, therefore allowing the counter to reach values as high as the fault diagnosis limit (here set to 30 which corresponds to $30\mu s$). As soon as the output counter reaches 30, the fault will be declared. Fault information is then used by the FPGA to reconfigure the topology by appropriately commanding the Triacs and switches.

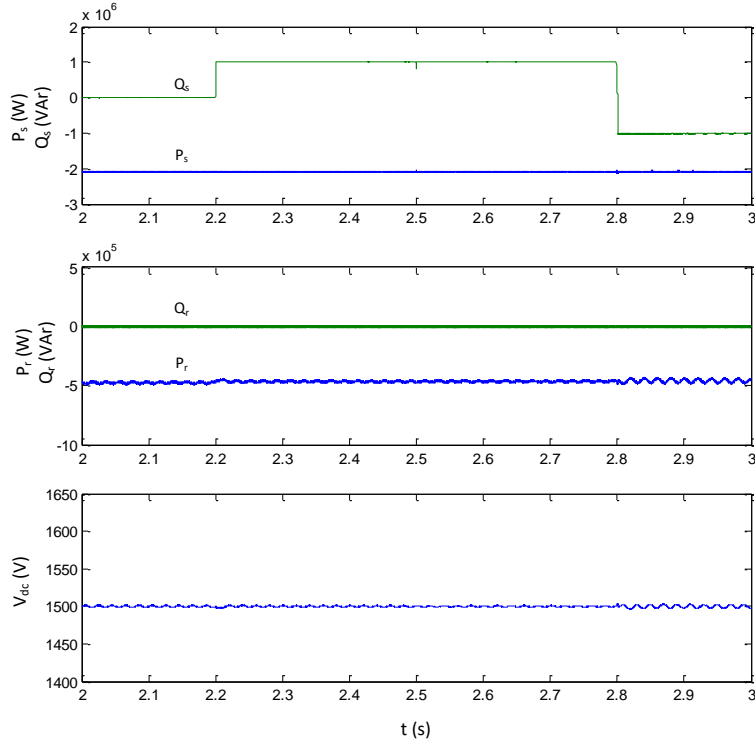


Fig. 5. Active and reactive stator and rotor powers and DC link voltage for an open-circuit switch fault in S_3 at $t=2.5$ s with fault detection and reconfiguration.

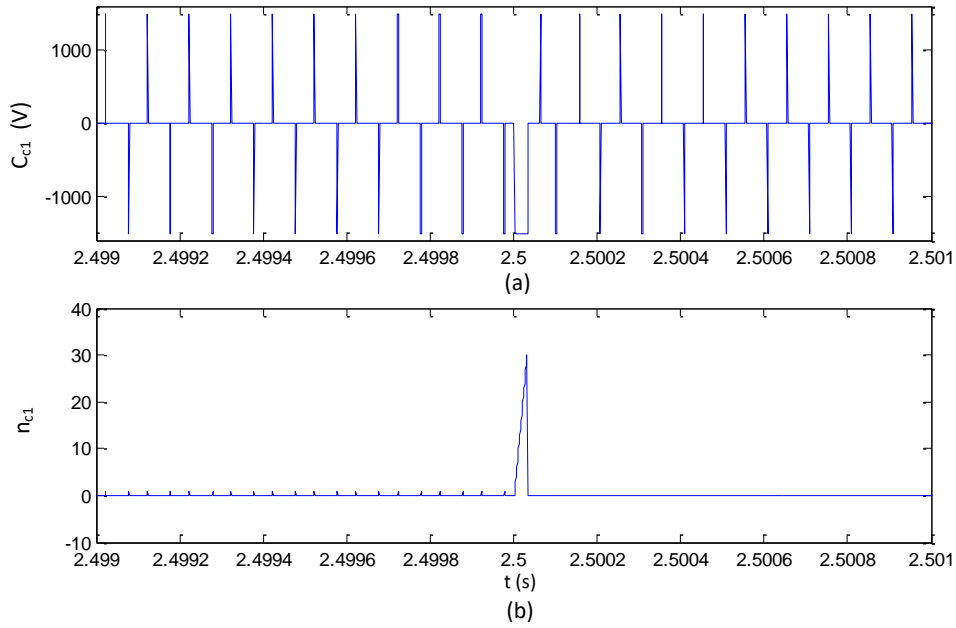


Fig. 6. (a) Voltage error between measured and estimated voltages; (b) fault diagnosis counter output.

Fig. 7 shows the stator and rotor currents. As it is visible, the fault effect has been negligible on these currents. The faulty phase current as well as Tr_{c1} current are shown in Fig. 8. After reconfiguration, the faulty leg current passes through this Triac and also in the remaining

- 1 diodes of the faulty leg which are now effectively in parallel with the diodes of the additional
- 2 leg.

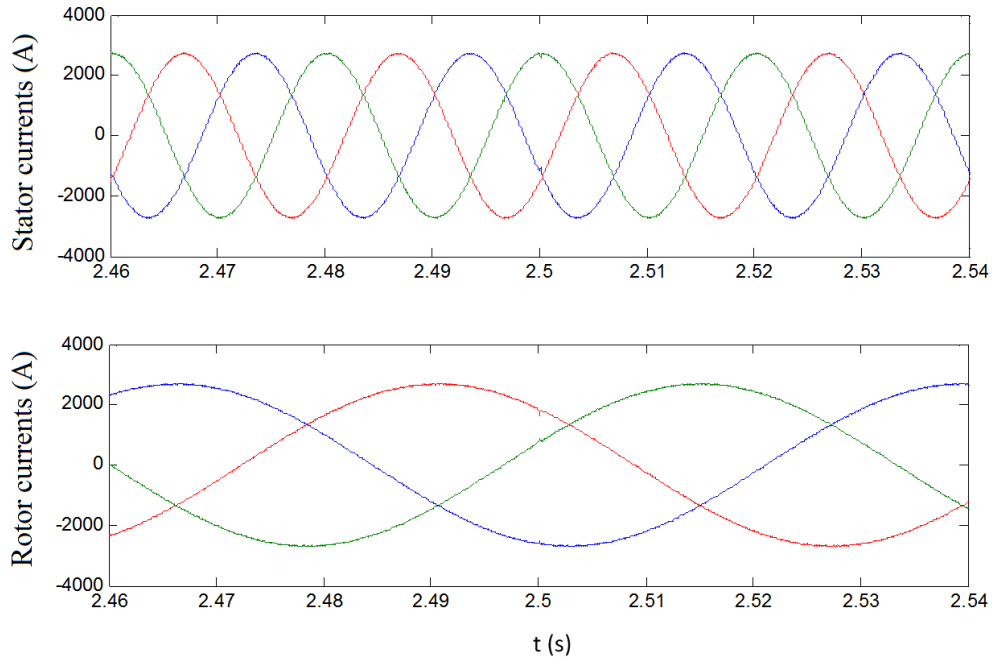


Fig. 7. Stator and rotor currents for a fault in S_3 .

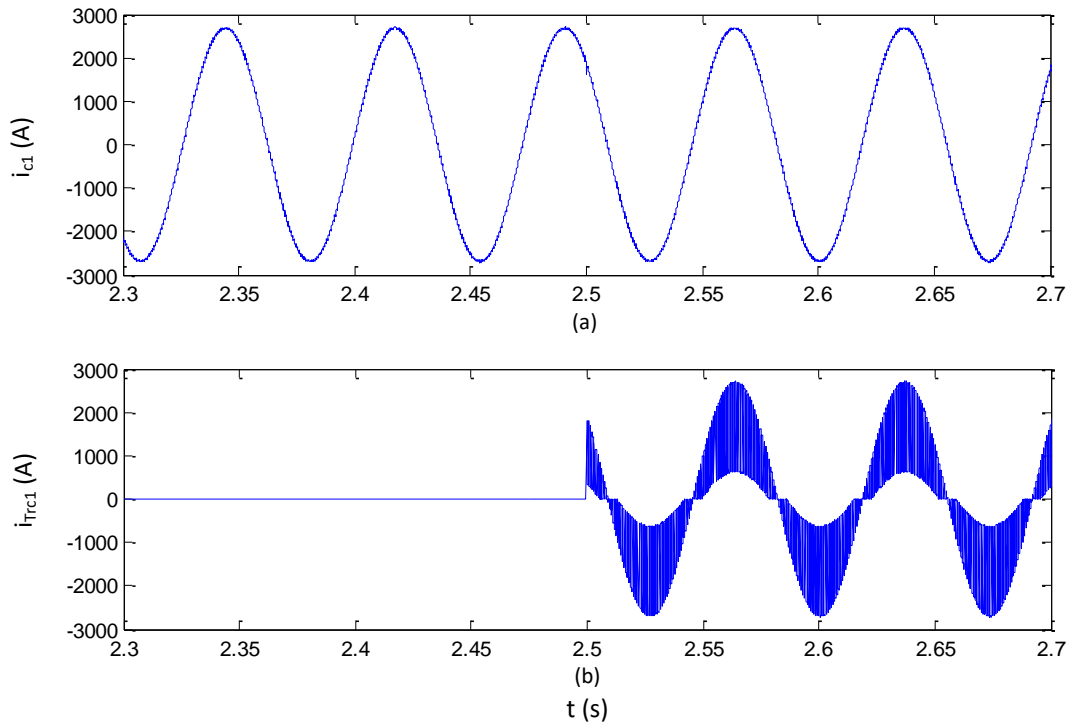


Fig. 8. (a) i_{c1} phase current; (b) i_{Trc1} Triac current.

An open-circuit switch fault in the GSC can also be similarly studied. Fig. 9 shows the GSC's active and reactive power as well as the DC-link voltage before and after a fault. Fault is again applied at $t=2.5$ s, but this time in S_3 , (Fig.1).

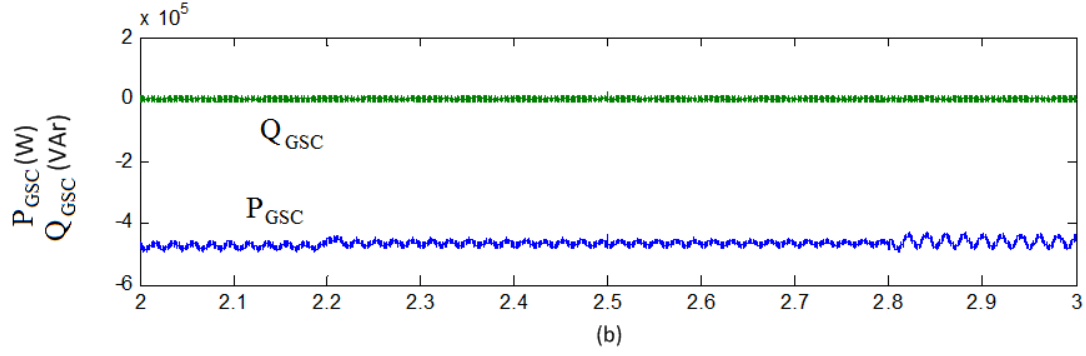
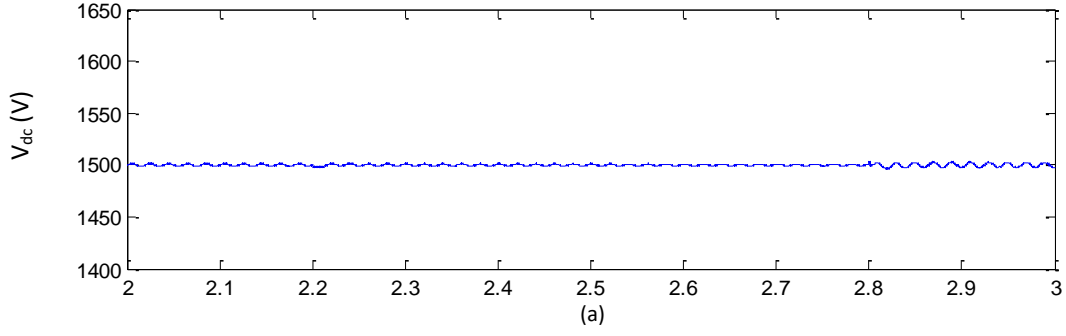


Fig. 9. Fault in S_3 , at GSC at $t=2.5$ s: (a) DC-link voltage; (b) GSC active and reactive powers.

Faulty leg's current and the corresponding Triac's current are also shown in Fig. 10.

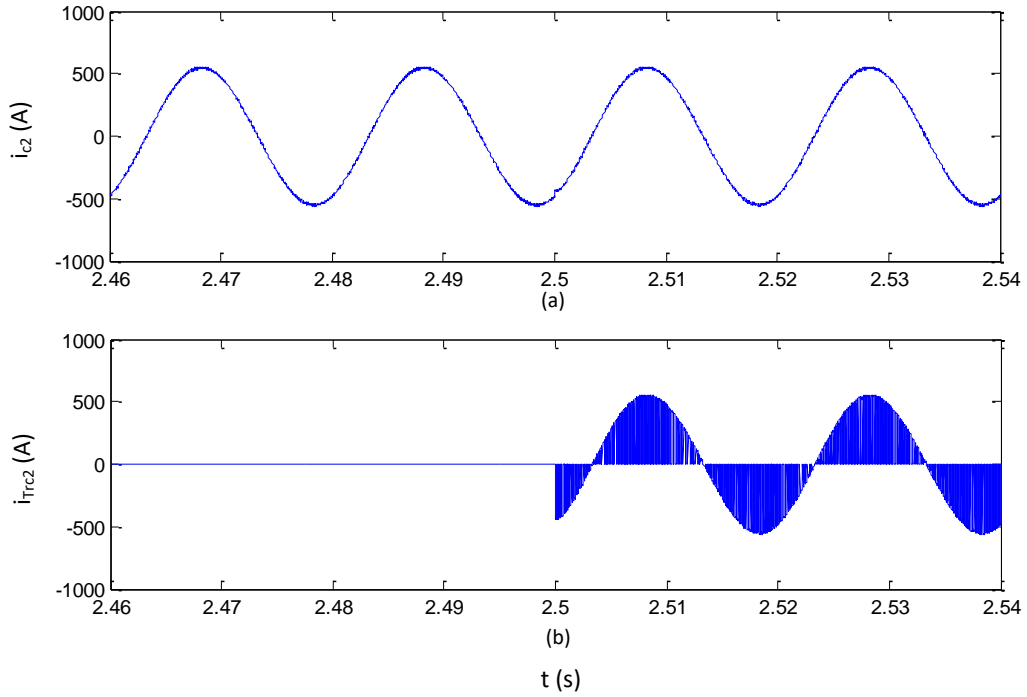


Fig. 10. Fault in S_3 , at GSC: (a) i_{c2} phase current; (b) i_{Trc2} Triac current.

HIL results have also been satisfying and in accordance with simulation ones, which shows that the FD algorithm and the controller can be used in an actual system. Since the HIL results have been similar to simulation results, they are not repeated here.

3.3. Experimental results

The control can be implemented on a proper digital device, such as a powerful microcontroller or DSP. Here, a DS1005 dSPACE is used for rapid prototyping. On the other hand, fault diagnosis algorithm must be carried out in parallel with other control tasks of the system, and must be very fast. Therefore, these devices are not the best options for implementation of the fault diagnosis and reconfiguration algorithm. This is mostly due to the fact that all of these processors execute their commands in a sequential manner, and provide limited overall bandwidth. Moreover, the waiting time for Interrupt Service Routines is one of their other shortcomings for this application. Therefore, logic level devices such as FPGA or CPLDs seem to be more suitable for implementation of the fault diagnosis algorithm. FPGAs allow very high speed calculations, and more importantly they are inherently parallel structured. Here for fault diagnosis, an Altera Stratix EP1S80B956C6 FPGA is used which includes 79040 logic cells, 12 programmable PLLs and 679 I/Os. Moreover, ADS7810U ADCs are used to convert the measured voltages from analog to digital.

Fig. 11 shows the implemented experimental setup. It is worth mentioning that the proposed fault diagnosis and reconfiguration does not depend on the system parameters, therefore a low or medium power lab setup can be used for these evaluations. A DFIG with 3 kW nominal power is coupled with a DC machine that emulates the wind turbine. Two three phase AC/DC converters from Semikron which use SKM50GB123D IGBTs and SKHI22A drivers form the PE stage. An additional leg (redundant leg) is added to one of the converters, using the same type of IGBT modules and drivers. Each converter is also equipped with a $2200\ \mu F$ capacitor. The converters are connected to the grid using a $3\ mH$ inductance with $0.4\ \Omega$ resistance.

FPGA sampling and step time is set equal to $1\ \mu s$, and dSPACE has a sampling time of $100\ \mu s$, equivalent to a switching frequency of 10 kHz. CV3-1200 voltage transducers and PR30 current clamps are used for voltage and current measurement, respectively. As mentioned in section 2.B, the choice of the parameter N in the FD algorithm depends on the system parameters. This depends directly on the total time delay in the control loop (including sensors, ADCs, FPGA, converters...). In the studied system, maximum total delay is calculated by adding the maximum delay of each of these elements, and is estimated to $13\ \mu s$. Therefore the fault observation time is chosen equal to $30\ \mu s$ because while it is considerably larger than that total delay, it still allows very fast fault diagnosis. In most practical cases, this value seems to be adequately larger than the total delay of the system, but if necessary, for specific systems it can be reduced. Considering a sampling period of $1\ \mu s$, N is then chosen equal to 30.

tests, stator active and reactive power references are set at 1 kW and 0 kVAr, respectively. Fault is artificially generated by setting the switching command of the driver to zero.

Fig. 12 shows the active and reactive powers before and after fault occurrence. Clearly fault diagnosis has been successful and smooth reconfiguration has taken place. Fig. 13 shows the rotor currents during fault occurrence and shows that they are not affected by the fault. Fig. 14(a) shows the details of fault detection. The fault occurrence moment is visualised when the fault signal goes from 1 to 0. This is in fact the signal that is multiplied in the gate signal of the faulty switch. As soon as fault occurs, the fault diagnosis counter starts increasing, and after 30 us, the fault is declared. Fig. 14(b) shows the faulty phase current, as well as the corresponding Triac's current.

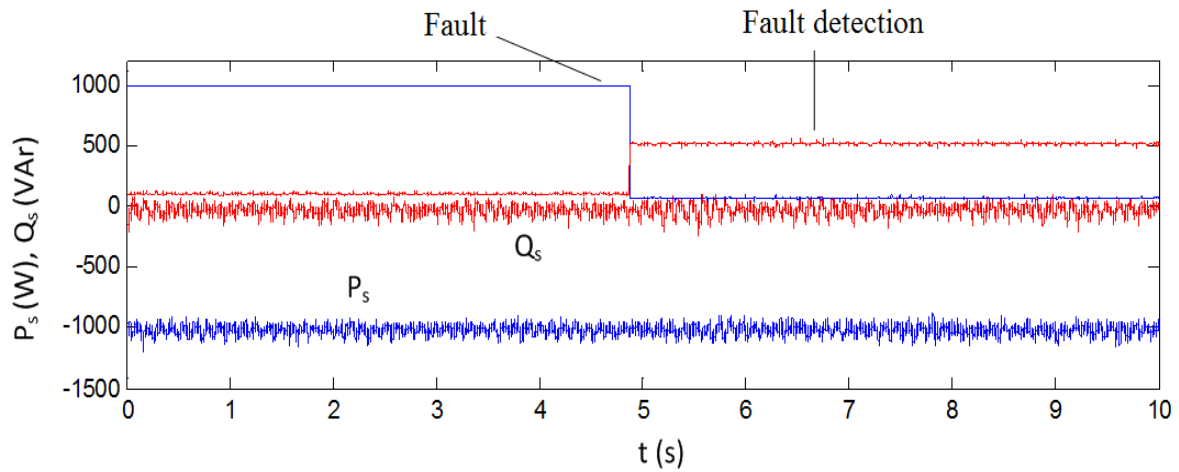


Fig. 12. Active and reactive stator powers before and after a fault in RSC.

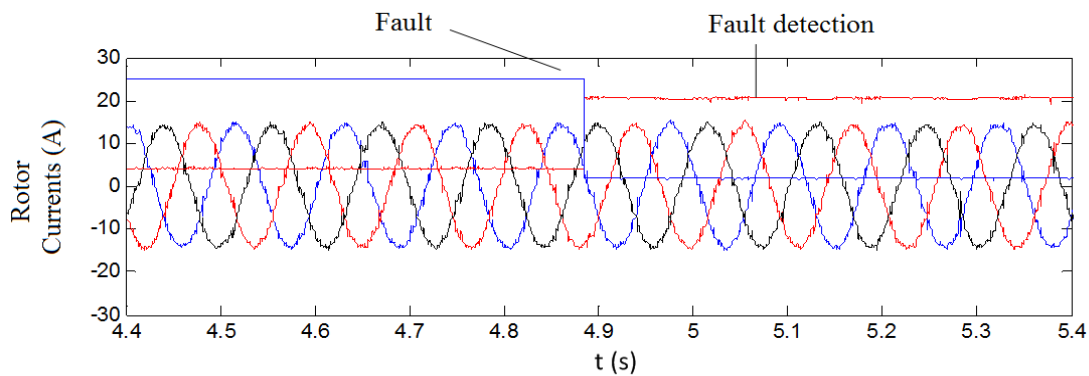


Fig . 13. Rotor currents for a fault in RSC.

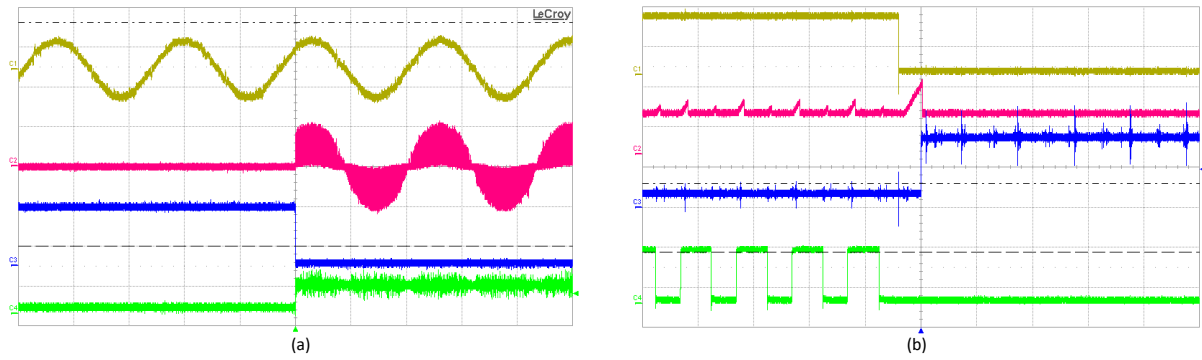


Fig. 14. Fault detection and reconfiguration for a fault in RSC: (a) from top to bottom: faulty phase current (20 A/div), Triac Tr_{c1} current (20A/div), fault signal, fault detection signal- time scale: 100ms/div; (b) detailed view of fault detection signals; from top to bottom: Fault signal, fault detection counter's output, Fault detection signal, switching command applied to S_3 (10V/div) - time scale: 100 μ s/div.

Similar tests are carried out for an open-circuit switch fault in the GSC (Fig.1). Fig. 15 shows stator active and reactive powers and Fig. 16 gives the GSC current before and after fault occurrence. Fig. 17 shows the fault detection signals and faulty phase and the corresponding Triac's currents. All these results testify that by using the proposed fault diagnosis and reconfiguration it is possible to detect a fault rapidly and guarantee the continuity of service in the WECS.

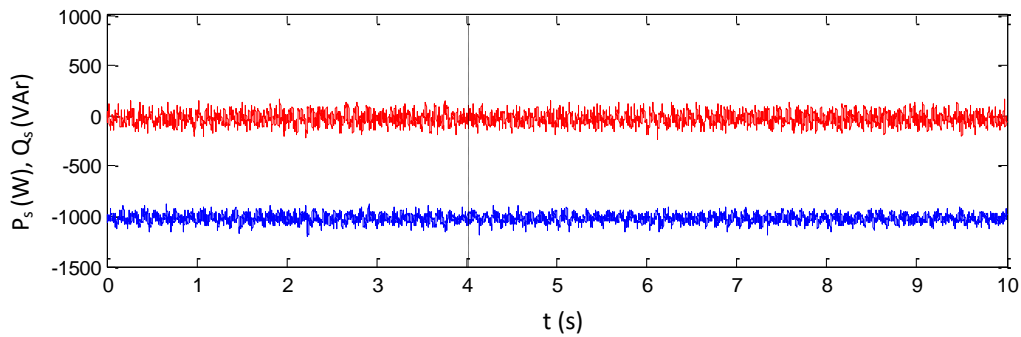


Fig. 15. Stator active and reactive powers for a fault in GSC.

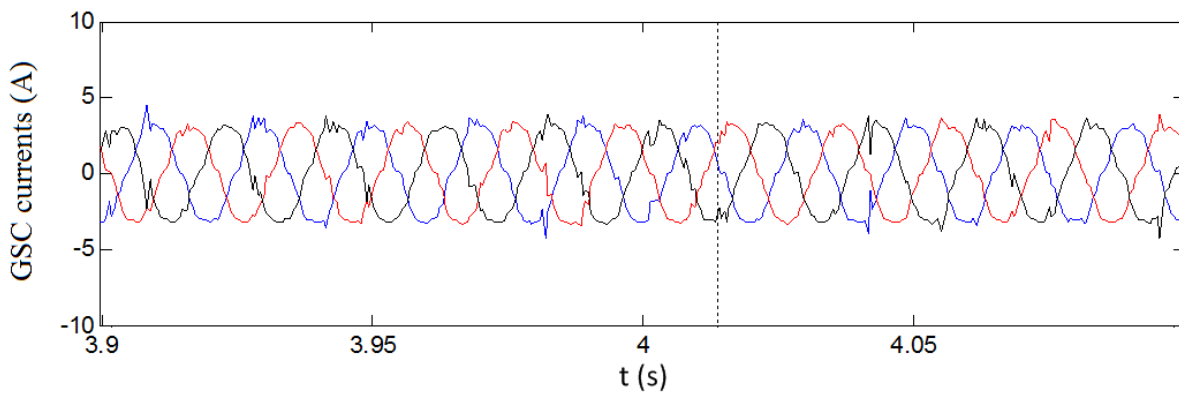


Fig. 16. GSC output currents for a fault in one of GSC's switches.

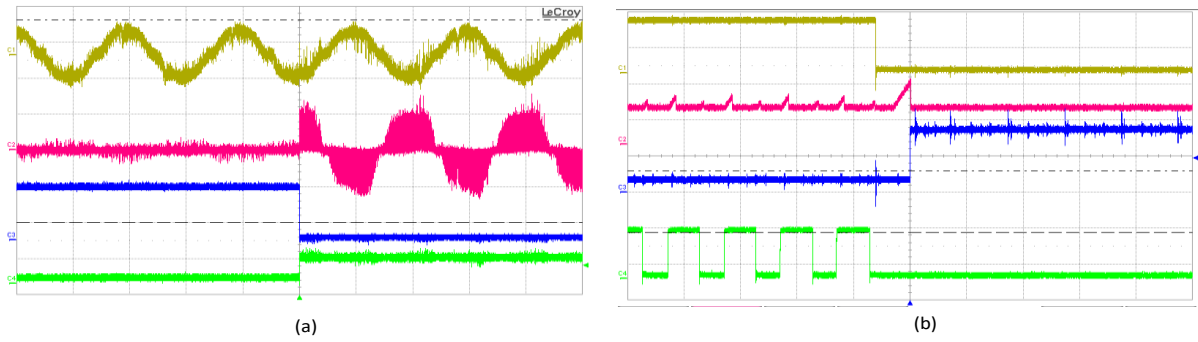


Fig. 17. Fault detection and reconfiguration for a fault in GSC: (a) from top to bottom: faulty phase current (5 A/div), triac Tr_{c1} current (5A/div), fault signal, fault detection signal- time scale: 10ms/div; (b) detailed view of fault detection signals; from top to bottom: Fault signal, fault detection counter's output, Fault detection signal, switching command applied to S_3' (10V/div) - time scale: 100μs/div.

In order to better evaluate the effectiveness of the proposed fault tolerant technique and fault detection method, Table III gives the comparison results with some of the existing methods in the literature. Using the proposed fault detection method, the fault can be detected faster than in other publications. Also, in the proposed fault-tolerant technique only two additional switches are required, while the rated power capability can be preserved in the post-fault operation. This is while other methods have drastic drop in their power handling capability in the post-fault mode, which can limit their operation range. Therefore the proposed method seems to be offering a good compromise between performance and cost.

Table III. Comparison of the proposed method with existing methods

Methods	Effectiveness	Detection time reported	Post-fault Output power	Additional components
Proposed method	Independent of rotor frequency and wind disturbances, same power output capability in post-fault mode	30μs	Rated power	Two IGBTs, 6 Triacs
Fault-tolerant T-type converter [12]	Limited operating range in post-fault mode,	Not discussed	Reduced power	No additional component
Fault-tolerant PMSG drive [13]	Limited operating range in post-fault mode	6 ms	Reduced power	One Triac
Fault-tolerant direct controlled PMSG drive [14]	Limited operating range in post-fault mode or necessary to oversize components	1.2 ms	Reduced power	Three Triacs
System reconfiguration under open-switch faults	Limited operating range in post-fault mode,	Not discussed	Reduced power	Six Triacs

in a doubly fed induction machine [16]				
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For future works, the effect of a second fault on the system and possibility of degraded mode operation in this case can be evaluated. Also, it might be interesting to see if it is possible to decrease the number of voltage measurement circuits, by using modern control techniques based on observers [28].

4. Conclusion

In this paper, a comprehensive fault tolerant power electronics interface for doubly-fed induction generator-based wind energy systems, including a robust and very fast open-circuit switch fault diagnosis is presented. First the whole system is modelled and simulations are carried out. In the second step the proposed fault diagnosis method and converter reconfiguration for post fault operation are validated through an approach called "FPGA in the Loop" from Hardware in the Loop family. The switch fault diagnosis method proposed in this paper is extremely fast, in comparison with other methods available in the literature. Moreover, the fault diagnosis is based on voltage rather than current measurement, and therefore is not sensitive to the operation conditions such as variable frequency of rotor currents and variable wind speeds. The fault-tolerant converter uses an additional leg which can replace a faulty one upon the fault diagnosis. Finally, as the proposed fault diagnosis and reconfiguration does not depend on the system parameters, therefore a low power lab setup is built for the experimental validations. The experimental results testify that by using the proposed fault diagnosis and reconfiguration it is possible to detect a fault rapidly and guarantee the service continuity of the studied wind energy system. Moreover, using the proposed method, it is possible to guarantee the same power capability of the system in the post-fault mode.

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